

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions:

1. (Currently Amended) A processor comprising:

a plurality of circuit blocks;

a plurality of local voltage regulators to each independently provide a local supply voltage to one of the plurality of circuit blocks, each of the plurality of local voltage regulators being co-located with the circuit block powered by the respective local supply voltage; and

a global power grid to power each of the plurality of local voltage regulators with a global supply voltage.

~~a voltage regulator to be powered by a first voltage and to provide a second voltage; and~~

~~a circuit powered by the second voltage.~~

2. (Currently Amended) The processor of claim 1, wherein at least one of the second voltage is local supply voltages is adjustable by the processor.

3. (Currently Amended) The processor of claim 2, wherein at least one of the plurality of voltage regulators ~~the voltage regulator~~ includes a digitized resistor to be set by the processor.

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4. (Currently Amended) The processor of claim 1, wherein at least one of the local supply voltages ~~the second voltage~~ is to be set to allow the respective circuit block to meet a timing requirement.
5. (Currently Amended) The processor of claim 1, further comprising a port to receive the ~~first~~ global supply voltage from an external voltage regulator.
6. (Currently Amended) The processor of claim 1, wherein at least one of the plurality of local voltage regulators ~~the voltage regulator~~ includes an op amp.
7. (Currently Amended) The processor of claim 6~~1~~, wherein at least one of the plurality of circuit blocks comprises ~~the circuit is~~ a digital circuit.
8. (Currently Amended) The processor of claim 1, wherein at least one of the plurality of circuit blocks ~~the circuit~~ includes at least a portion of a core of the processor.
9. (Currently Amended) The processor of claim 1, wherein at least one of the plurality of circuit blocks ~~the circuit~~ includes a memory region.
10. (Original) The processor of claim 9, wherein the memory region is a cache.

11. (Currently Amended) A computer system comprising:

a discrete voltage regulator to provide a global supply voltage V_{ee}; and

a processor including

a plurality of circuit blocks,

a plurality of local voltage regulators to each independently provide a local supply voltage to one of the plurality of circuit blocks, each of the plurality of local voltage regulators being co-located with the circuit block powered by the respective local supply voltage, and

a global power grid to power each of the plurality of local voltage regulators with the global supply voltage.

~~a local voltage regulator to be powered by the global V_{ee} and to provide a local V_{ee} for the processor.~~

12. (Currently Amended) The computer system of claim 11, wherein at least one of the local supply voltages ~~the local V_{ee}~~ is adjustable by the processor.

13. (Currently Amended) The computer system of claim 12, wherein at least one of the plurality of local voltage regulators ~~the local voltage regulator~~ includes a digitized resistor to be set by the processor.

14. (Currently Amended) The computer system of claim 11, wherein the processor includes a cache to be powered by at least one of the local supply voltages ~~the local V_{ee}~~.

15. (Original) The computer system of claim 11, wherein the processor is a graphics controller.

16. (Currently Amended) A method comprising:

providing a global supply voltage to a plurality of local voltage regulators through a global power grid, each of the plurality of local voltage regulators being co-located with one of a plurality of circuit blocks within a processor; and

independently providing a local supply voltage from each of the plurality of local voltage regulators to power a respective one of the plurality of circuit blocks.

~~providing a first voltage to a processor comprising an integrated voltage regulator;~~

~~powering the voltage regulator with the first voltage, the voltage regulator to provide a second voltage; and~~

~~powering at least a portion of the processor with the second voltage.~~

17. (Currently Amended) The method of claim 16, wherein independently providing the local supply voltages comprises:

adjusting at least one of the local supply voltages further comprising adjusting the second voltage by the processor.

18. (Currently Amended) The method of claim 16, wherein ~~powering at least a portion of the processor includes powering one of the circuit blocks~~ comprises a

floating point unit of the processor, and wherein independently providing the local supply voltages comprises powering the floating point unit.

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